

Preliminary Data

Dual Core Industrial Controller DCIC 9907

Product Brief (Rev 0.43)

The Dual Core Industrial Controller (DCIC 9907) is a System-on-Chip (SoC) designed as the central digital element of a Servo System Platform.

Although optimized for motion control applications, the DCIC 9907 key features lead to a wide variety of industrial applications, like

- Field bus controller node
 - CAN 2.0B
 - Ethernet PowerLink
- Field bus to Ethernet Network bridge/ firewall, gateway
 - TCP/IP
 - Web server
 - Firewall
- Real-Time Ethernet control node
 - EPL Manager Node (Master) or Control Node (Slave)
- Real-Time data acquisition and measurement
 - High precision timer capture/compare unit
 - Three phase PWM output
 - Intelligent serial ADC and DAC interface to external analog front-ends

1. Key Features

The main integrated on-chip functions of the DCIC 9907 are:

- 128 MHz Host ARM core, combining an ARM946E-S core, 16kbyte I-Cache, 4kbyte D-Cache, 32kbyte I-TCM (tightly-coupled memory) and 8kbyte D-TCM
- 128 MHz Control ARM core, combining an ARM946E-S core, 16kbyte I-Cache, 4kbyte D-Cache, 32kbyte I-TCM and 4kbyte D-TCM
- Multi-layer AHB interconnection scheme for high system throughput
- Standard IEEE 1149.1 (JTAG) interface access to both ARM cores
- Extended debug facilities via 8-bit port embedded trace macrocell (ETM) for Host ARM core
- On-chip static memory of 97kbyte divided into two banks of 96kbytes and 1kbyte
- Two interrupt controllers, each one dedicated to one ARM core with:
 - Support for 32 interrupt sources
 - Support for up to 16 interrupt vectors
 - Hardware interrupt priority
 - AHB mapped for faster interrupt response
 - Software interrupt generation possible
 - Interrupt request (IRQ) and fast interrupt request (FIQ) generation
- DMA controller:
 - Dual AHB Master
 - Eight DMA unidirectional channels
 - 16 DMA request lines
 - Single and burst DMA request signals
 - Memory-to-memory, memory-to-peripheral and peripheral-to-peripheral transfers
 - Scatter or gather DMA is supported through the use of linked lists

- Synchronous Static Memory Controller:
 - Up to eight independently memory banks for static memory-mapped devices (SRAM, ROM, Flash-Eprom, Burst-ROM support)
 - Contains an AHB test interface controller (TIC)
 - Little-endian operation
 - 8, 16 or 32-bit wide external data paths supported
 - Programmable bus cycle characteristics, independently for each memory bank
- Two 10/100 Mbit Ethernet MACs with HW-extension for real time protocols
- Two controller area network (CAN) controller:
 - CAN protocol version 2.0 part A and B
 - Programmable bit rate up to 1 Mbit/s
- Four independent universal asynchronous receiver transmitter:
 - Programmable baud rate generator
 - 16*8-bit transmit FIFO, 16*12-bit receive FIFO
- Four independent synchronous serial interfaces:
 - Programmable serial communication protocols (Motorola SPI, TI SSI and National Semiconductor Microwire)
 - 8*16-bit transmit FIFO, 8*16-bit receive FIFO
- Versatile motion control peripheral block:
 - Programmable time synchronisation unit
 - Programmable pulse width modulation (PWM) unit
 - Encoder evaluation unit
 - Complete, configurable interface to connect analog front ends with synchronous serial communication
 - Three auxiliary PWM outputs
- Up to 109 general purpose I/Os (partly shared with dedicated functions of other peripherals)
- 15 external Interrupt inputs
- Watchdog Timer (16-bit programmable counter)
- Five-channel 16-bit general purpose timer
- On-chip clock generator with PLL

2. System Architecture

The DCIC 9907 provides two ARM946E-S™ cores, named Host and Control ARM. Both differ only in the sizes of their tightly coupled memories. Furthermore the Host ARM core supports ARM's real-time trace technology with the addition of the 8-bit port embedded trace macrocell (*ETM*).

The ARM946E-S™ is a synthesizable macrocell well suited to a wide range of embedded applications. It combines an ARM9E-S™ CPU with flexible instruction and data caches, instruction and data tightly coupled memory (TCM) interfaces, a protection unit, and an AMBA bus compliant AHB interface. The size of the instruction and data cache and instruction and data TCM memories of each core is tailored to the application.

The Control ARM core is aimed to execute almost all program code out of its fast TCM. The fastest control loops may reside in TCM, whereas the core's cache ensures high throughput while external memories are being accessed.

The Host ARM generally controls the various communication channels, where the use of a RTOS and larger code sizes are expected. The Host core's cache is tailored for higher instruction and data throughput.

Both cores implement the ARMv5TE instruction set and feature an enhanced 16 x 32-bit multiplier capable of single cycle MAC operations, and 16-bit fixed point DSP instructions to accelerate signal processing algorithms and applications.

The architecture of the dual ARM processor system is based on the AHB interconnect matrix. This enables parallel access paths between multiple standard AHB master and slave modules in a system. It is achieved by using a more complex interconnection matrix and gives the benefit of increased overall bus bandwidth.

In the DCIC 9907 a six master/four slave interconnect matrix is implemented. Both of the ARM processor cores, the Ethernet MACs or the DMA masters may get access to one of the four slave channels. While the

static memory controller and the main internal static RAM block each are connected directly to one interconnect slave port, the other slave devices of the system are grouped into two AHB buses and connected to the matrix. Because most of the peripheral cores like the CAN modules and most of the ARM compatible peripherals are implemented with an APB-interface, additional AHB to APB bridges are necessary. Simultaneous access conflicts from multiple masters to a single slave are resolved by a fixed AHB-Master prioritization incorporated in the interconnect matrix.

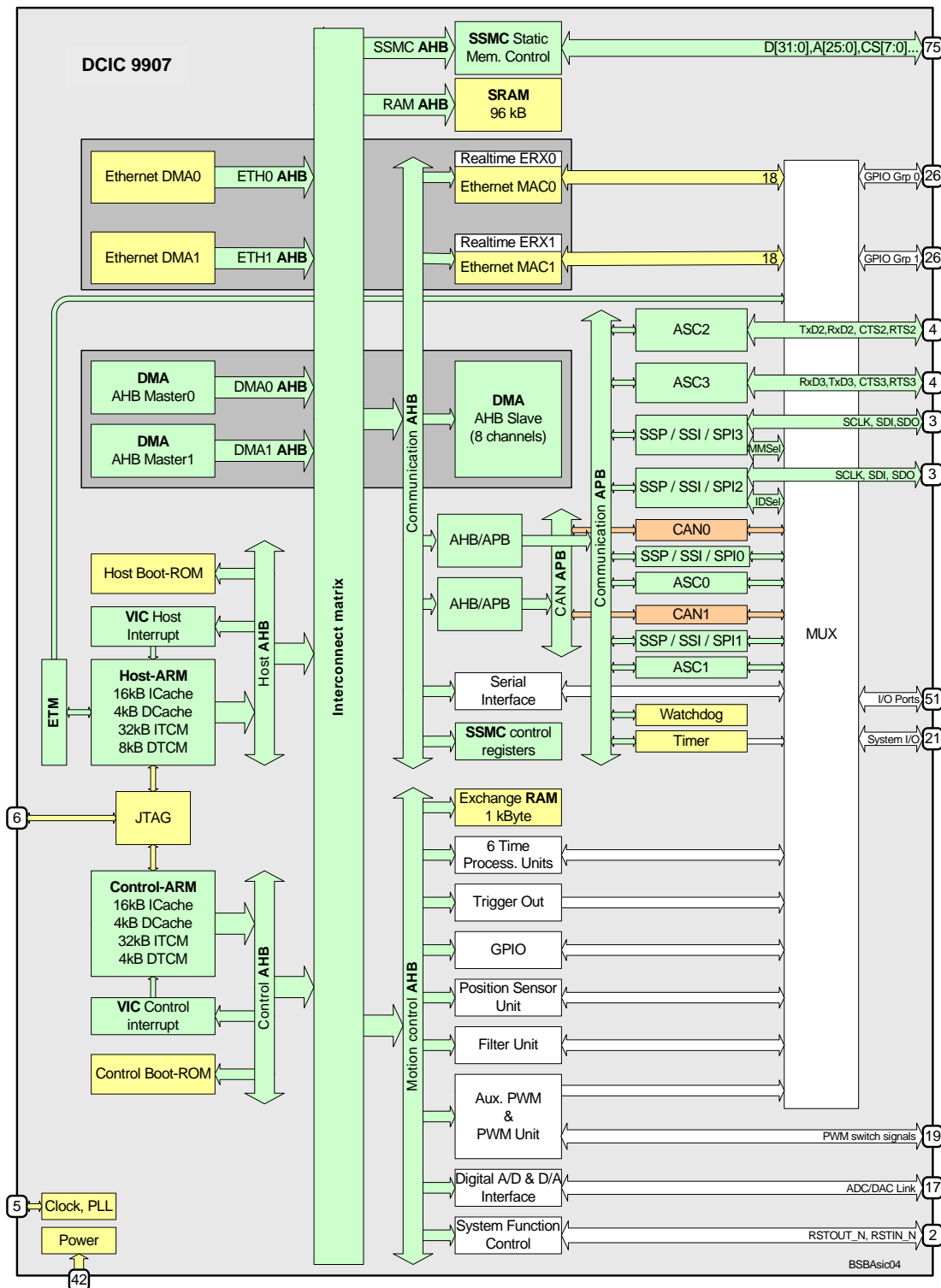


Figure 2-1: DCIC 9907 Functional Block Diagram

Via the implemented synchronous static memory controller (SSMC) it is possible to extend the internal memories through external static memory devices like Flash-ROM or SRAM in standard or burst mode.

Different bus modes with different characteristics are independently programmable to allow a wide variety of external devices, each with its own dedicated chip select. Up to eight chip selects are programmable.

For high speed data throughput two blocks of SRAM are integrated. One 96 kbyte zero waitstate memory supports the Host ARM's data flow. This range is cacheable in its data cache. Dedicated to the data exchange between Host and Control ARM a smaller SRAM block of 1kbyte is implemented separately. With this the data accesses of the Control ARM are decoupled from possible fill cycles of the Host ARM's Data cache lines.

The demand for powerful and flexible communication interfaces is supported by numerous communication IP-blocks. The functionality of blocks Ethernet *MAC0* and *MAC1* is improved by certain hardware extensions. This supports the ARM processor's algorithms and supervisory functions and allows the system to perform in real time environments.

For a more flexible applicability of the DCIC 9907 there are several internal functions that can be attached to external pins by configuration. One multiplex block is implemented to gate the signals from the internal components to the pins. Most of the communication peripherals and dedicated functions may be routed in that way.

The on-chip boot code enables the DCIC 9907 to fetch instructions from external SPI devices (e.g. memories) at system start-up.

The *Motion Control Peripheral (MCP)* block contains the peripherals and interfaces especially needed for motion control applications. The application timing and synchronization of the DCIC 9907 is implemented here. Furthermore a complete interface to a power stage, including a three phase programmable PWM unit, and an encoder evaluation unit with a serial communication interface to position sensors is realized. For a flexible external connection of different analog to digital and digital to analog converters a configurable serial interface with different communication modes (Motorola SPI or ADS7869/VECANA02) is included. Finally most of the dedicated peripheral signals may be shared on the external pins with general purpose input output (GPIO) ports. This is programmable via configuration registers.

3. Physical Characteristics

- 1.8 V internal, 3.3 V external operation
- TTL compatible I/O pins
- Full performance extended temperature range (-40 to +85 C)
- 304-pin plastic ball grid array (BGA), 1,27mm ball pitch

4. Motion Control

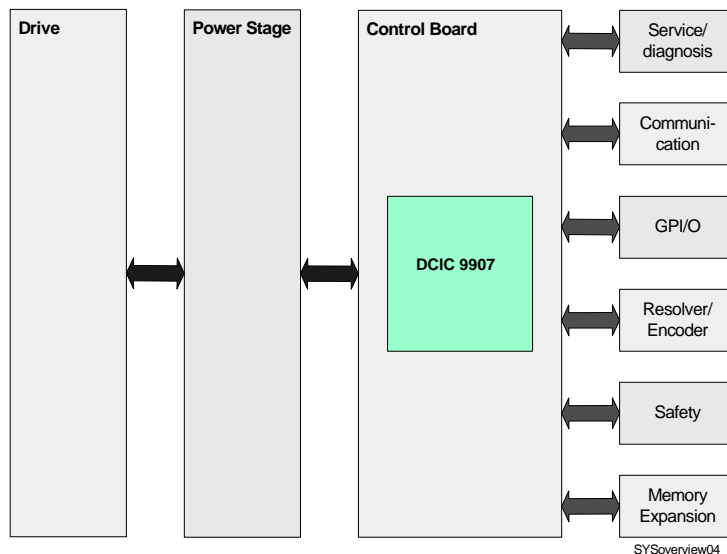


Figure 4-1: Servo System Platform Overview

The DCIC 9907 as the main part of the control board is optimized for high performance AC drive controls. Beside the dedicated interface to the power stage of a three phase inverter there are several interfaces to interact as a complete industrial control. Figure 4-1 depicts a typical servo control architecture based on the DCIC 9907.

Additionally to the extensive motion control peripheral set several on-chip peripherals from standard components like timer, DMA and interrupt controller up to high performance communication peripherals like two 10/100 Mbit Ethernet MACs are implemented.

As a conceptual goal, the system can be expanded by up to four expansion modules. The SoC ideally supports a glueless interface and flexible functional configuration towards these modules. One module slot is designed to expand the device for safety-critical applications. The memory expansion slot enhances PLC functionality like large non-volatile storage. Finally, two module slots are prepared to interface to high-speed, real-time communication links and field busses as well as other peripherals like position sensors, digital inputs, etc.

5. Industrial Datacom

With its numerous communication interfaces, an industrial network controller or bridge can be designed with minimal overhead.

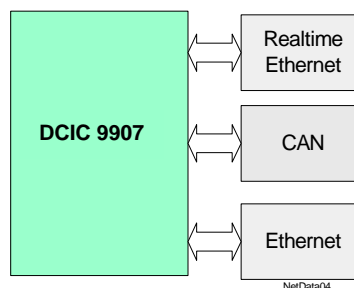


Figure 5-1: Industrial Network Controller

6. Data Acquisition and Processing

Versatile digital interfaces to external SPI-compliant analog front-ends and the ability to process incoming and outgoing data in real-time, the DCIC 9907 may serve as the central controller for real-time data acquisition and data processing.

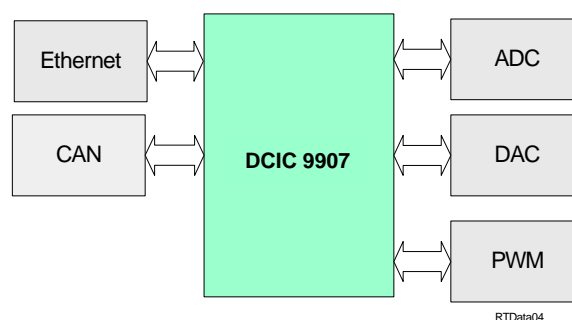


Figure 6-1: Real-Time DAQ and Processing

7. Specials

- ETM traceport is shared with user I/O
- Power-saving feature. Some components are held in reset by software controllable register to save power. (Exit by HW-reset only.)
- Boot-ROM Address mapping externally controlled.

- Inter-connect Matrix: Priorization and access control of the 6 AHB-masters to grouped AHB paths maximizes data throughput. Access from different AHB-masters to slaves on separate AHB-slave paths can be made in parallel.

8. Clock requirements

The external clock (about 16 MHz to 40 MHz) is expected at FIN. An external PLL is used to multiply the input clock to obtain 256 MHz. All other clocks are derived from that source.

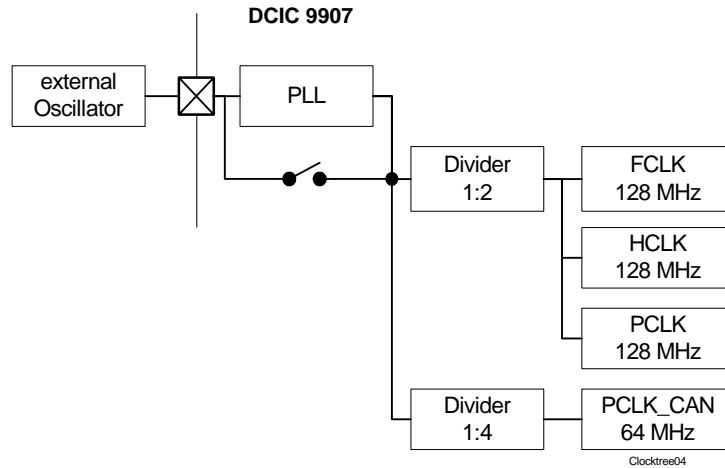


Figure 8-1: Clock requirements

Special care should be taken to ensure maximum data throughput (ARM cores, DMA master IF, Ethernet MACs). This implies usage of cache.

All internal peripherals are accessed with zero AHB waitstates @ 128 MHz (in case no access conflict occurs). Motion control logic block (MCP) is accessible with 0 (for writes) and 1 (for reads) waitstates. SSMC operates on full HCLK frequency, thus MEMCLK to external synchronous memories is also 128 MHz by design.

9. How to reach us

For more information about the DCIC 9907 and the services and support available for them contact us:

DualCore Semiconductor GmbH

Campestr 12
D-90419 Nuernberg

+49 911 338 433
+49 721 151 314 835

www.DualCore.com
info@DualCore.com

Trademarks

ARM, Thumb, ETM9, ARM9E-S are registered trademarks of ARM Limited. All other products, brands or services mentioned herein may be trademarks of their respective owners.

Other

Information in this document is provided solely to enable system and software implementers to use the described product. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

DualCore reserve the right to make changes without further notice to any products herein. DualCore makes no warranty, representation or guarantee regarding the suitability of this product for any particular purpose, nor does DualCore assume any liability arising out of the application or use of any product or circuit, and specifically disclaim any and all liability, including without limitation consequential or indirect damages. "Typical" parameters that may be provided in DualCore documentations can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. DualCore does not convey any license under its patent rights nor the rights of others. DualCore products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended or support or sustain life, or for any other application in which the failure of the DualCore product could create a situation where personal injury or death may occur. Should Buyer purchase or use DualCore products for any such unintended or unauthorized application, Buyer shall indemnify and hold DualCore and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages and expenses and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that DualCore was negligent regarding the design or manufacture of the part.

Copyright

This document is copyrighted by DualCore. It may not be published or redistributed without written permission of DualCore.

History

01	Oct-21 2003
02	Nov-04 2003
03	Feb-19 2004
03a	Dec-07 2004
03b	Jan-31 2005
04	Mar-15 2005
041	Jun-07 2005
042	Oct-24 2005
043	Jan-07 2006